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Optimization of Power Dissipation in CMOS Circuits Utilizing w/l Parameter of the Sleep Transistor

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Abstract—*In majority of the event driven applications, circuits spend most of their time in an idle state where no computation is being performed. This is termed as the stand-by mode and the sub-threshold leakage power during this phase is a clear blot on the circuit's performance. The use of MT (Multi-threshold)-CMOS technology has been very effective in the implementation of circuits with high performance and low power consumption. This paper sees the use of sleep transistor to gate the power supply lines for the entire module. The size of sleep transistor (essentially an NMOS transistor) is synthesized based on mutually exclusive discharge patterns of the individual gates in the circuit. The analysis further revolves around the use of W/L of the sleep transistor as a parameter for the sleep transistor so as to study the effects of its variation on total power dissipation and propagation delay (switching speed) of the proposed module.*

Index Terms*: MTCMOS, Sleep transistor, w/l ratio.*

1. INTRODUCTION

The aim is to minimize static power dissipation in the stand-by (sleep) mode and this is achieved through a power gating technique. This is usually being implemented in a low power design. The reduction of power supply voltage is one of the most widely practiced measures for low power design. While such reduction is usually very effective, several important issues must be addressed so that the system performance is not sacrificed. In particular, reducing the power supply voltage leads to an increase of delay. There are three main sources power dissipation in CMOS circuits:

- *Dynamic Power Dissipation*: due to the charging & discharging of load capacitor driven by the gate.
- *Short-Circuit Power Dissipation*: occurs when gate switches.
- *Leakage Power Dissipation*: due to reverse biased leakage on the transistor drains, & sub-threshold leakage through the channel of the device.

The main area of concern is the leakage power dissipation, which leads to the wastage of power even when the circuit is not switching. Several methodologies have been proposed so as to tackle this limitation and the standout has been the MT (Multi-Threshold) CMOS technique.

The MTCMOS technique involves the use of high-V_T transistors so as to gate the power supply lines and the ground connections of the module. These transistors are operated in the ON state when the actual CMOS logic is in the active mode so that the CMOS logic operates with low switching power dissipation and small propagation delay. These are kept OFF when the CMOS logic is in the stand-by mode and thus, the conduction paths for any sub-threshold leakage currents that may originate from the internal low-V_T circuitry are effectively cut-off. A sleep transistor (usually an NMOS) is used to gate the module. Its use is justified as it can be closely modeled as a resistor which helps in the delay analysis of the circuit.

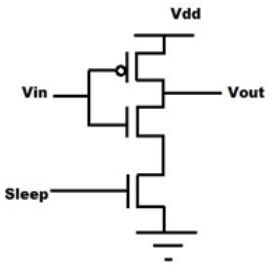

Figure-1(a) MTCMOS Inverter.

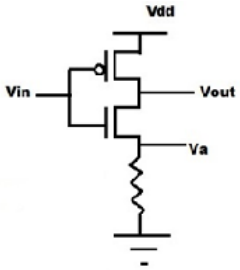

Figure-1(b)Equivalent MTCMOS in active mode.

2. APPROACH TO TRANSISTOR SIZING

Instead of searching for the worst case input vector for the worst case discharge patterns in the circuit, we analyze mutual exclusive discharge patterns. For this we ensure that every individual gate meets a local performance constraint so that any combination of gates in a path will also meet the performance requirements. Each individual gate is assigned its

own high voltage sleep transistor whose size will be locally determined through exhaustive simulations. Once sized with individual sleep transistors, we can systematically merge the sleep transistors together which are shared among mutually exclusive gates. Finally, these sets of sleep transistors can then be combined to make a single sleep transistor for the whole circuit that guarantees that for any input vector the circuit performance will be within the specified range of degradation.

3. SIMULATION IN A SERIES OF STEPS

In order to achieve the best results, one should initially use a detailed simulator like TANNER EDA to simulate as large a block as possible and to exhaustively determine the optimal sleep transistor size. Next, the hierarchical merging technique can then be applied to these existing blocks to synthesize an overall sleep transistor for a larger module, where determining a worst case input vector would have been exceedingly difficult. Applying this hierarchical methodology too early can result in unnecessary overestimates for sleep transistor sizes.

STEP (1)

As a start, series of inverters are considered as a digital circuit. Different arrangements are formed for the sleep transistor to connect with:-

1. Series of inverters, with even numbered connected to sleep transistors.
2. Series of inverters, with odd numbered connected to sleep transistors.
3. Series of inverters, all connected to sleep transistors.

For these arrangements, temperature is chosen as parameter and it is varied from 20ºC to 120ºC and the corresponding variations in voltage drop, current, power, delay across sleep transistor(resistor) are estimated.

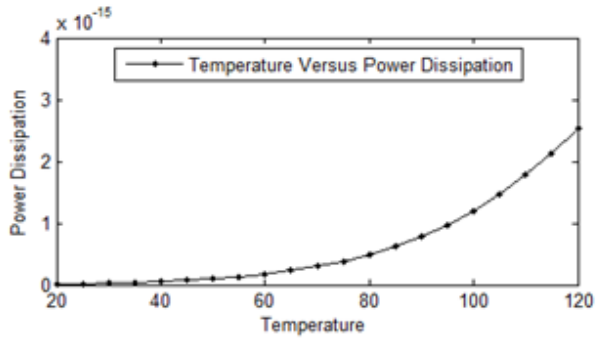

Figure- 2.

The analysis results in the conclusion that power dissipation increases with temperature rise but is considerably reduced as compared to the circuit without sleep transistor as can be seen from figure(2).

STEP (2)

NAND gate is used to form a sequential circuit and simulated for different parameters in following steps:-

1. Six NAND gates; even numbered gates connected to sleep transistor.
2. Six NAND gates; odd numbered gates connected to sleep transistor.
3. Six NAND gates; all of them connected to sleep transistor.

Sleep transistor	NAND no.
Sleep1	2,4,6
Sleep2	1,3,5
Sleep3	1,2,3,4,5,6

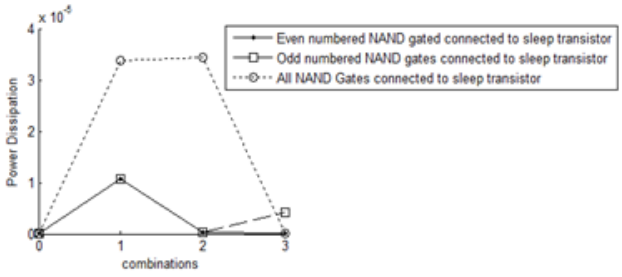

Figure- 3.

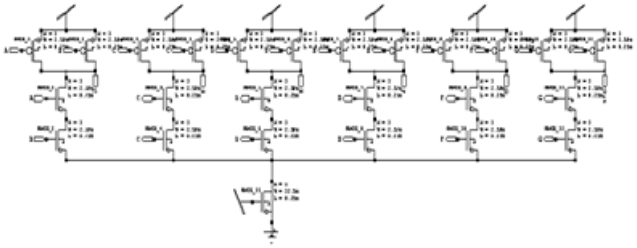

Figure- 4.

Results of the clustering were analyzed and the worst results were found when all the NAND gates were connected to sleep transistor. Further this sequence was tested by replacing individual sleep transistors to each gate by a single sleep transistor, which is operated in the modes ON and OFF. The sleep ON signifies the active mode of the circuit and thus analyzes dynamic power dissipation and propagation delay while sleep OFF signifies the stand-by mode of the circuit to calculate the static power dissipation of the proposed module.

STEP (3)

The above form of the circuit which involved six NAND gates connected to a single sleep transistor was treated as a template and it was tested for a striking parameter of the sleep transistor size i.e. w/l. The variation of W/L involved increasing W whereas keeping L fixed so as to vary the range from 10-100 and the corresponding variations in the power dissipation and propagation delay were observed.

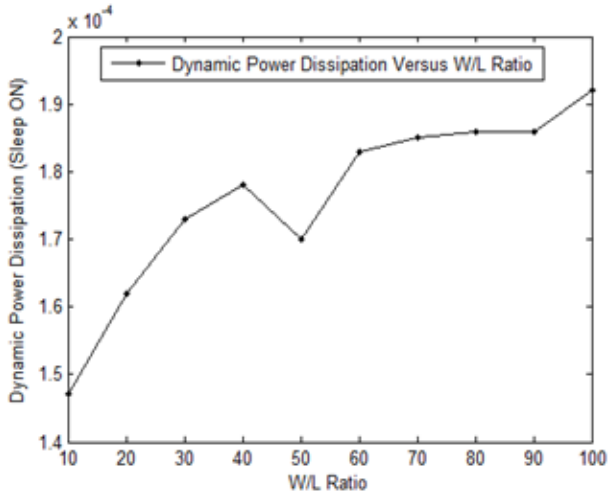

Figure- 5.

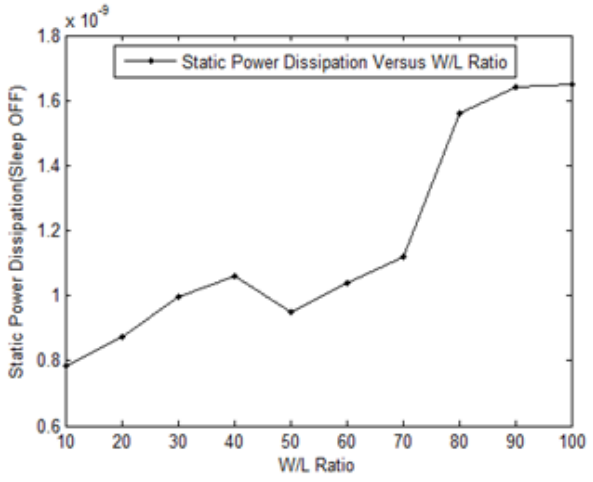

Figure- 6.

4. RESULTS

By replacing n sleep transistors with a single one, the sub-threshold leakage current decreases and the parasitic capacitance on the virtual ground increases. It provides an upper bound on the sleep transistor size to guarantee better performance by placing delay constraints on individual blocks. It is most useful when applied to a large module in conjunction with a detailed simulator for sizing. Further the variation of w/l as a parameter in order to study the variations in switching power dissipation and propagation delay result in a trade off such that if we desire less power consumption then we would have to settle for a higher propagation delay at low w/l. On the other hand, the requirement of low propagation delay would trade off power dissipation at a higher w/l ratio for the sleep transistor. This can be seen in conjunction with the following mathematical equations:-

$$P_{total} = \propto_T . C_{load} . V_{DD}^2 . f_{CLK} + V_{DD} (I_{shortcircuit} + I_{leakage} + I_{static})$$

$$t_{propagation} = \frac{C_{load}}{K(V_{DD} - V_T)}$$

$$K = u . C_{OX} . w/l$$

The above equations indicate a direct dependence of power dissipation and propagation delay on w/l of the sleep transistor. With increasing w/l, the leakage current increases which in turn increments the power dissipation while with increasing w/l, the parameter K increases and results in the decrement of propagation delay.

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